REMARKS

Claims 1-13 are pending in the application.

Claims 1-7 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Civanlar et al., (USP 5,691,768) and further in view of Anderson (USP 6,275,507).

Claims 8-13 are allowed.

Analysis of the Rejection

Regarding the rejection of claims 1-7, Applicant submits that it would not have been obvious to combine the teachings of Civanlar et al. and Anderson t al. as proposed by the Examiner, and even if the teachings were to be combined, the present invention would not have been obvious. One reason for this is that the references, taken alone or in combination, fail to teach or suggest the claimed feature of:

> sequentially switching to decode a predetermined unit of a bit stream for each of the other plurality of channels, by obtaining a program state corresponding to a program counter value associated with a respective one of the plurality of channels

In rejecting the claims, the Examiner admits that "Civinlar fails to disclose that the syntax processor obtains a program state corresponding to a program counter value associated with a respective one of a plurality of channels." The Examiner states, however, that "Anderson discloses a transport demultiplexor (Anderson: column 8, lines 29-35) with a syntax processor that obtains a program state corresponding to a program counter value associated with a

respective one of a plurality of channels (Anderson: column 9, lines 40-60) in order to maintain stream continuity (Anderson: column 10, lines 15-25)." Applicant submits that Anderson does not teach or suggest obtaining a program state corresponding to a program counter value, and that the Examiner, in interpreting the term "program counter", so as to encompass the continuity counter of Anderson, is interpreting this term beyond the generally accepted meaning in the art.

In more detail, the term "program counter" is a term of art which should not be interpreted as broadly as the Examiner has interpreted this term.

The term "program counter" has long been used in the art to indicate a register which stores the address of the next instruction (or part thereof) to be executed. For example, in the textbook "Microprocessors and Programmed Logic", by Kenneth L. Short, a program counter is defined as follows:

> The program counter is an operational register that always holds the address of either the next instruction to be executed or the address of the next word of a multiword instruction that has not been completely fetched. In either case, at the completion of the execution of any instruction, the program counter contains the address of the first word of the next instruction to be executed. The operational nature of the program counter allows its contents to be implemented by the control unit.

"Microprocessors and Programmed Logic", Second Edition, by Kenneth L. Short, 1987, p. 69 (copy enclosed).

A Google search of the term "program counter" provides definitions consistent with that in the above quoted book. For example, the first "hit" (at http://en.wikipedia.org/wiki/Program_counter provides the following definition:

> The **program counter** (also called the **instruction pointer**, part of the **instruction sequencer** in some computers) is a register in a computer processor which indicates where the computer is in its instruction sequence. Depending on the details of the particular machine, it holds either the address of the instruction being executed, or the address of the next instruction to be executed. The program counter is automatically incremented for each instruction cycle so that instructions are normally retrieved sequentially from memory. Certain instructions, such as branches and subroutine calls and returns, interrupt the sequence by placing a new value in the program counter.

The cited portion of Anderson et al. merely teaches incrementing a **continuity counter**, presumably to ensure that the packets are processed in order. This is different from the claimed feature of using a **program counter** value for decoding. Using the program counter value, as claimed, causes the processing to move to a specific point in the **program** whose execution results in the decoding. This is a very different concept than counting packets to make sure that all packets are sequentially processed, as in Anderson et al.

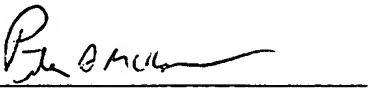
In view of the accepted meaning of the term "program counter" as evidenced by the above definitions of "program counter", Applicant respectfully submits that the Examiner's interpretation of Anderson, as this reference applies to the claim language "obtaining a program state corresponding to a program counter value associated with a respective one of the plurality of channels", goes beyond the art recognized definition of the term "program counter." That the Applicant intended to not deviate from the usual meaning of the term "program counter" is

evident in the description of the preferred embodiment of the invention, for example, at page 7, lines 8-13.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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